

# A Programmable FSK-Modulator in 350nm CMOS Technology

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**Abstract**—This paper describes the design of a programmable FSK-modulator based on VCO and its implementation in 0.35μm CMOS process. The circuit is used to transmit digital data at 100Kbps rate in the frequency range of 400-600MHz. The design and operation of the modulator is discussed briefly. Further the characteristics of PLL, frequency synthesizer, VCO and the whole design are elaborated. The variation among the proposed and tested specifications is presented. Finally, the layout of sub-modules, pin configurations, final chip and test results are presented.

**Keywords**—FSK Modulator, CMOS, VCO, Phase Locked Loop, Frequency Synthesizer.

## I. INTRODUCTION

FSK modulators are widely used in digital signal communication. The basic idea is to transform the digital information into analog signals of two different frequencies. One frequency is used to transmit logic 0 and the other for logic 1. Usually, the FSK modulators use a set of fixed frequencies. But, the present paper presents a unique architecture in which the set of frequencies can be varied using external input. The PLL-based designs usually attenuate the high frequency data and some information may be lost [1]. A binary frequency-shift keying (BFSK) signal can be defined by

$$[s(t) = \begin{cases} A \cos 2\pi f_0 t & 0 < t < T \\ A \cos 2\pi f_1 t & \text{elsewhere} \end{cases} \quad (1)$$

Where A is a constant,  $f_0$  and  $f_1$  are the transmitted frequencies and T is the bit duration. An M-ary frequency-shift keying (M-FSK) signal can be defined by

$$[s(t) = \begin{cases} A \cos(2\pi f_i t + \theta) & 0 < t < T \\ 0 & \text{elsewhere} \end{cases} \quad (2)$$

For  $i = 0, 1, \dots, M - 1$ . Here, A is a constant,  $f_i$  is the transmitted frequency,  $\theta$  is the initial phase angle, and T is the symbol duration [2, 3]. A considerable research work has been performed by various researchers on power-performance and area optimization of PLL-based FSK modulators. [4] has presented a 6.5GHz BFSK modulator suitable for wireless sensor applications, achieving 22mW power consumption with 20μs start-up time. In [5], the authors have implemented an FSK modulator with a MEMS switch to select one of the two resonators with different resonant frequencies.

In this paper we will present the design of a fully integrated 400-600MHz frequency synthesizer and FSK modulator. The main objectives are to reduce the cost by reducing the effective

chip area and power consumption. The circuit is designed, implemented and tested with 350nm CMOS technology and 3.3V supply voltage.

## II. SYSTEM DESIGN AND OPERATION

The block diagram of the whole system is as shown below.

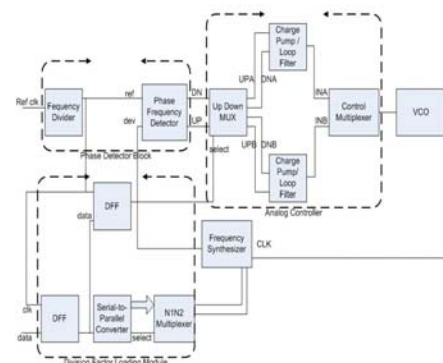


Fig. 1: FSK Modulator Block Diagram

The basic operation of an FSK-modulator is to transform an input digital signal into a set of frequencies consisting of two frequency values, one of them is used for logic 1 and the other for logic 0. The PLL-based modulator is composed of the following main components.

### A. Phase Frequency Detector (PFD)

The primary purpose of the PFD is to simply measure the difference in phase and frequency between both signals and produce an output that is proportional to the difference. Since the objective of the PLL is to ensure that the feedback signal is equal to the reference signal, the PFD commands the rest of the PLL to either lower or raise the frequency coming out of the Voltage Controlled Oscillator (VCO). This is accomplished by either using its up or down output. Signals from the up output instruct the VCO to increase the frequency and / or phase while signals from the down output perform the opposite. Phase detector can be designed by a number of ways. The simplest of them is an XOR function whose operation is shown in figure 2.

Phase detectors can also be designed using edge-triggered D-flip flops but it is not a proportional detector, and also affects the timing of the control loop [6]. We have designed a sequential phase detector having two output signals Up and

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Manuscript received April 19, 2010; revised June 24, 2011.



Fig. 2: XOR Phase Detector

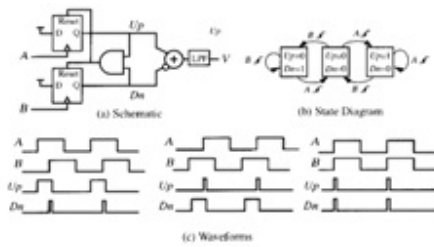


Fig. 3: Phase Detector Waveforms

Down. A generic design of a three state sequential detector is shown in the following figures.

When a positive edge is received on A (B), Up (Dn) is latched high and held until a positive edge is received on B (A), at which point AND resets both the flip-flops. A brief pulse, proportional to the circuit delays, appears on Dn (Up), as the flip-flops are reset. If A leads B, Up goes high for a time proportional to the phase difference between A and B. If B leads A, the roles of Up and Down are reversed. If the two inputs A and B are exactly in phase, brief pulses of equal width are produced on both Up and Down. These short pulses are important for avoiding a dead band in this phase detector [6]. This detector has a wider range of detection  $\pm 2\pi$ . The detector also works for phases out of its range. If the phase angle between A and B approaches  $2\pi$ , the detector still continues to interpret the phase angle as positive due to the memory in the additional third state. Due to its extended behavior, the sequential phase detector is also able to detect the frequency difference [6]. Suppose, if clock A has a higher frequency than Clock B, Up pulses will provide an average voltage proportional to the frequency difference, while the Down pulses will average near 0, as shown below. That's why this detector is also referred as Phase/Frequency Detector (PFD).

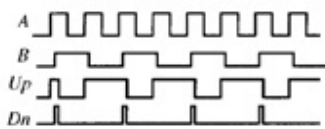


Fig. 4: Phase and Frequency Detection

The sequential PFD is not subject to false lock problem of the flip-flops and possesses a large capture range [6].

**B. Charge Pump Loop Filter**

In our design, we have implemented a block called Analog Controller, which consists of two analog multiplexers and two charge pump loop filters. This block controls the dynamics of whole the loop. The loop filter not only filters the high

frequency components from the PFD output but also regulates the loop dynamics. Active RC loop filters are not suitable, in various prospects, to be implemented on-chip. This is because; the high gain low output impedance amplifier consumes a huge chip area as well as the power. Also it is very difficult to fabricate high-value linear capacitors and resistors with reasonable tolerance. Normally an N-well JFET is used as a resistor. Variations in resistance tolerance and temperature coefficients also deteriorate the FET parameters. In order to control the loop dynamics efficiently, we have used a charge pump loop filter whose model is shown in figure 5.

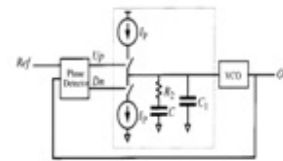


Fig. 5: Charge Pump Loop Filter

The frequency and transient responses of a charge pump loop filter are exactly the same as those of active loop filter. However, the charge pump filter eliminates the need for a high performance operational amplifier. Instead the amplifier is substituted by a switched current source [6]. The loop transfer function, oscillation frequency and damping factors are derived as follows.

$$\frac{\phi_{out}}{\phi_{in}} = \frac{\phi_{out}}{\phi_{out} + \phi_E} = \frac{\frac{I_p \cdot K_{VCO}}{2\pi C} (R_2 C + 1)}{s^2 + \frac{I_p \cdot K_{VCO}}{2\pi} \cdot R_2 s + \frac{I_p \cdot K_{VCO}}{2\pi C}} \quad (3)$$

$$\omega = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{R_2 \cdot C}} \quad (4)$$

$$\gamma = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{R_2 \cdot C} \cdot \frac{R_2 \cdot C}{2}} \quad (5)$$

Where  $K_{VCO}$  and  $K_{PD}$  are the VCO and phase detector gains and  $\phi_E$  is the phase error.

When the PLL locks at a certain frequency, the mismatches between the Up and Down pulling current sources and the mismatches in the switching devices, produce ripples at the output control voltage. The ripples cannot be removed from the PLL due to resistor R2 and hence VCO output is modulated and jitter is produced. Capacitor C1 is introduced for filtering of ripples at the output [6].

**C. Voltage Controlled Oscillator**

The key component of a phase locked loop is a VCO, which takes a control input  $V_f$  and produces a periodic signal with frequency

$$f = f_c + k_f \cdot v_f \quad (6)$$

Where,  $f_c$  is the centre frequency of the VCO and  $k_f$  is the gain with the unit hertz per volt [6]. The gain determines the frequency range and stability. Depending on the input from the other PLL components, the VCO creates a frequency that matches the reference signal. A VCO can be implemented

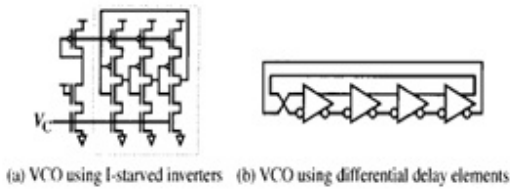


Fig. 6: VCO Implementation

using current-starved inverters or differential delay elements as shown in the diagrams [6].

Figure 11 shows the variation of VCO frequency with the controlling voltage.

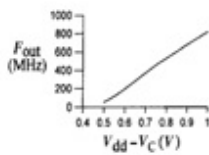


Fig. 7: VCO Voltage vs Frequency

D. Frequency Divider

The basic function of the Divider, which is a part of the feedback loop, is to reduce the frequency from the VCO into a value that can be comparable to the Reference Signal.



Fig. 8: A Basic Frequency Multiplier

In this design, a chain of T Flip Flops are used to create a divider. The division factor of the Divider depends on the equation  $2^n = \text{divide by } n$  where  $n$  is the number of T Flip Flops used. The frequency of the VCO is divided down in a modulo-N counter and compared and locked to a reference at  $f_0$ . Thus the VCO output is multiplied and locked at  $N \cdot f_0$ . In [7], the designers have designed the divider block using a combination of current mode logic (CML) and CMOS static logic. They have used divide-by-2 and divide-by-2/3 blocks for high frequency division.

E. Frequency Synthesizer

The frequency synthesizer (FS) produces output frequencies which are integer multiples of the reference frequency. An FS produces an output frequency  $f$ , which is the reference frequency  $f_r$  multiplied by the division ratio  $N$ , that is

$$f_{out} = N \times f_r \tag{7}$$

Since  $N$  is an integer, the output frequency must therefore be restricted to whole multiples of  $f_r$ . If we interpose a fixed Prescalar with a value  $V$ , we can drop the output frequency

easily into the operating range of the divider  $N$ . However, we have now introduced a Prescalar factor ( $V$ ) into the equation, so the output frequency is now

$$f_{out} = V \times N \times f_r \tag{8}$$

The scaling factor of Prescalar ( $V$ ) is much greater than 1 in most cases so it is not possible to generate every desired integer multiple of the reference frequency  $f_r$ . The solution is Dual Modulus Prescalar. Dual-modulus means that it can divide by two different factors, usually  $V$  and  $V+1$ , which factor to apply is changed using a control input.

F. Division Factor Loading Module(DFLM)

The DFLM is used to convert the serial data (the division factor for the Frequency Synthesizer) to parallel data, and load it to the Frequency Synthesizer. The DFLM consists of the following sub blocks Serial to Parallel Converter (SPC) and Division Multiplexer (DM).

III. CIRCUIT SCHEMATICS

The schematics of some of the building blocks of our design are shown below. All the circuits have been designed and simulated in Cadence 0.35μm tool.

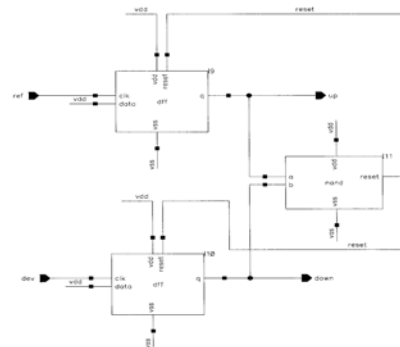


Fig. 9: Phase Detector

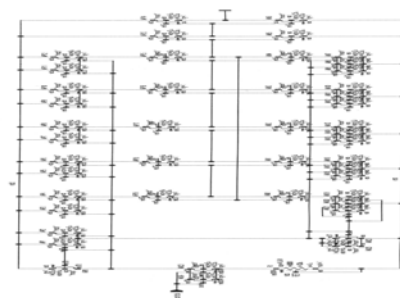


Fig. 10: Phase Detector

IV. LAYOUT DETAILS

All the circuits have been designed, simulated and then layout prepared for each sub-module. Then all of the modules are integrated together and simulated again. After that, the

TABLE I: VCO Process Parameter Simulation

Process Parameter	@900mV	@3.3V
cmostm	102.76MHz	556MHz
cmoswp	211MHz	556MHz
cmosws	60MHz	403.55MHz
cmoswo	169MHz	415.45MHz
cmoswz	84.36MHz	610MHz

whole design is integrated with PAD-frame assembly. The PADs are selected carefully for each signal. Then a final simulation is performed which also includes the parasitic effects of the PAD frame and the load coupling capacitances. Figure 11 shows the layouts of VCO and PFD.

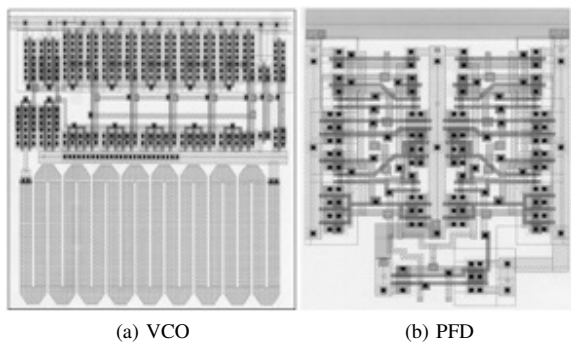


Fig. 11: VCO and PFD

## V. SIMULATION RESULTS

The designs have been verified for each module and sub-module from system level to layout level, using Cadence 350nm design suite. The VCO is the most critical component of the whole design. Hence, it is tested for different CMOS parameters as shown in table 1. The simulation results are shown in figure 12.

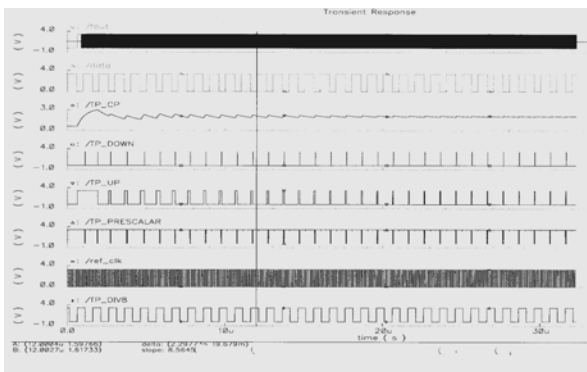


Fig. 12: Simulation Results at Layout Level

## VI. EXPERIMENTAL RESULTS

The snapshot of the fabricated chip is shown in figure 13. The position of FSK modulator is in the bottom right part of the chip. The chip has been tested and verified after fabrication. The following parameters are achieved.

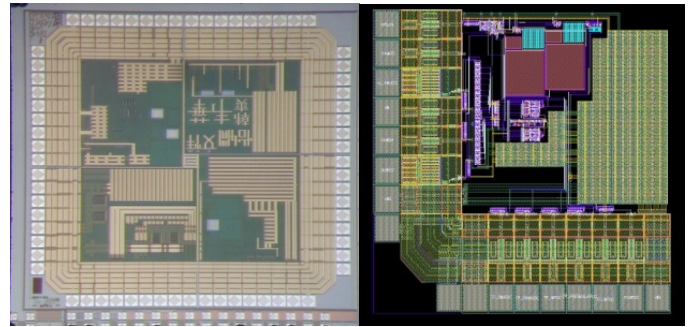


Fig. 13: Full Chip Microscopic View

Power supply voltage: 3.3 V  
 All components integrated on chip  
 Center frequency: 403 MHz  
 Modulation input: 100 kbit/s  
 Modulation frequency max: 1 MHz  
 Power consumption: 22mW  
 Chip design area: 1.2 mm<sup>2</sup>  
 Chip core area: 700μm x 800μm = 0.56 mm<sup>2</sup>  
 Total project pin count: 17  
 Total off-chip test points: 06  
 On.chip current densities: less than 1 mA/μm

## VII. CONCLUSION

This paper demonstrated the design of a 400-600MHz PLL-based programmable FSK modulator and its implementation in 350nm CMOS process. The total core area covered by the design is 1.2mm<sup>2</sup> with 17 pinouts and 22mW power consumption at 3.3V supply. The proposed design offers the possibility of varying the modulation frequencies by loading an external dividing factor serially. The design is suitable for low cost medium frequency range applications.

## ACKNOWLEDGMENT

We are thankful to Dr. Atila Alvandpour, Dr. Martin Hansson and Henrik of Linkping University, Sweden, for their support and cooperation during this research. We also thank Austria Microsystems for sponsoring the chip fabrication of our design work.

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