DWDM Optical Supervisory Channel by Manchester Code on FPGA

Hossein Borhanifar, Ali Poureslami, Seyed Ali Alavian

***Abstract*—**The next generation optical wavelength division multiplex (WDM) network will transport a stupendous aggregate data rate that consists of all existing types of payload, synchronous and asynchronous, and all types of traffic, voice, video and internet. The Optical Supervisory Channel (OSC), which is an important section in every DWDM system, carries voice and data between sites for monitoring and controlling all specifications in the system. This paper describes a complete OSC circuitry implemented in a FPGA (Field Programmable Gate Array) chip. High density and speed of FPGA chips cause that we can implement accuracy requirements of the design. Using of Manchester code in the plan achieves some beneficial features such as non saturation in optical receiver modules, better synchronization and error detection in optical communication. The design focuses on precision and maximum throughput in an OSC board.

***Keywords*—**DWDM, OSC, Optic, Manchester Code, FPGA

I. Introduction

DENSE WDM or DWDM is a leading technology for extremely demanding networking solutions. The “density” refers to the closeness of the technology’s signal frequencies to one another. DWDM platforms typically support all point-to-point and ring topologies, as well as a wide range of transmission distances. The technology can potentially transmit over hundreds or even thousands of kilometers using proper amplification and dispersion management techniques. Because DWDM is completely protocol-independent and transparent, it can carry any transport protocol, including SONET, SDH, storage protocols, data, video, and other types of transmissions.

Most metro DWDM platforms support up to 32 protected, or redundant, wavelengths, providing enormous density and scalability. Organizations can further increase density using service aggregation. Service aggregation supports multiple service types per wavelength for efficient transmission. This flexibility enables companies to efficiently maximize the carrying capacity of all of their wavelengths over a single pair of fiber, lowering the total cost of ownership and reducing equipment requirements.
The information such as data and voice of every site are transported to all the amplifier sites through an OSC (Optical Supervisory Channel) signal in the same fiber having a wavelength of 1,510 nm. The OSC provides an out-of-band, full-duplex communications channel for remote node management, monitoring and control similar to the Data Communications Channel (DCC) of SONET/SDH. The OSC for network management and control is optically separate from user data (wavelengths). So even if the OSC is lost, data forwarding continues uninterrupted.

Equipped with its 1510 nm MUX/DEMUX filter, the OSC travels the same fiber as the DWDM stream and always terminates on neighboring nodes. Because it has a dedicated wavelength, the OSC data is entirely independent of the user data. The OSC is implemented as a point-to-point carrying a 2.048 Mb/s used for inter-nodal management and control.

Implementing of all OSC features can be done with a FPGA chip that the plan is described in the paper.

Hossein Borhanifar is with the Electrical Engineering Department, Islamic Azad University, Nazar Abad Branch, Tehran, Iran (e-mail: h.borhanifar@kiau.ac.ir).

Ali Poureslami is with Department of Optical Communication, Iran Telecom Research Center ITRC, Tehran 1439955471, Iran (e-mail: poureslami@itrc.ac.ir)

Seyed Ali Alavian is a Member of Faculty, Department of Electrical Engineering, University of ICT, Tehran, Iran (e-mail: alavian@ictfaculty.ir)

II. Features of Designed OSC Capabilities

- Dual-SFP Transceiver Compatible with 120Km Transmission Length
- Voice Connection (Point to Point & Conference)
- Voice Alignments (No Sync, Busy, Wrong, Free, Ring Back Tones)
- Pulse and Tone Dialling, Caller ID
- Compatible with conventional Telephone Set
- Settable Variable Numbering (101 ~ 115)
- Data Connection:
  Throughput ability:
  - 1slot=64 kbps ~ 29slot=1856 kbps
  - Implemented 4slot=256 kbps
- Quad Buffer for west/east, send/receive
- Fully pack/unpack Supervisory frame in each station
- Manchester code and decode on transmit and receive
- Fully low voltage design (3.3V)
- Housekeeping Alarm handling Ability
- Bit Error Rate Measurement Ability

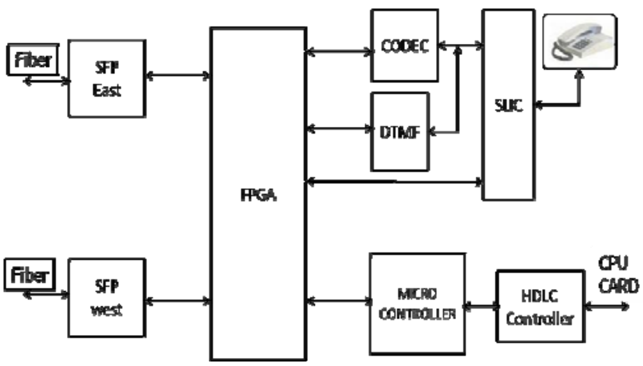

Fig. 1 Block diagram of the OSC board

Fig. 1 represents a block diagram of the OSC board. Voice is provided via SLIC and CODEC circuitries and there is a DTMF component for Tone Dialing and caller ID features. In other side, data which is provided by CPU card is received by HDLC controller and a microcontroller. Both voice and data are integrated in a FPGA chip. The EP2C5TC144-8 is a cyclone family of Altera's devices. This component, which includes 4780 logic cells, 127876 memory bits, 2 PLL's and 26 multipliers, is choice for our design. Voice, data and all required signals are transmitted and received by circuits in the FPGA. Every OSC board has communicates with 2 DWDM systems which are located in east and west sides. So each board has two SFP for optically communicate with east and west stations.

III. Different Functions in the FPGA

The diagram in the Fig. 2 shows different functions in the FPGA device.

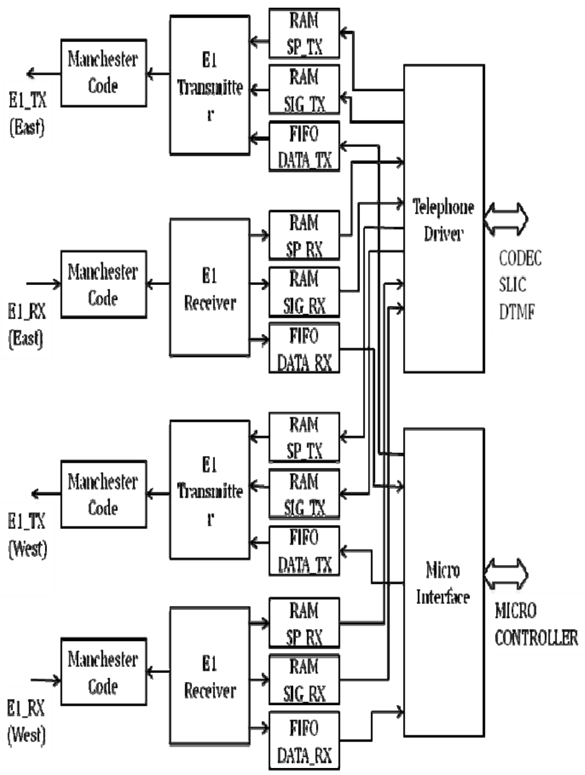

Fig. 2 The diagram of all blocks in the FPGA

A. Telephone Driver

The telephone driver block controls voice and required signals about telephone. The voice can be as point to point or conference connection. It also supports voice alignments such as no sync, busy, wrong number, free and ring back tones, that every one actives in own special situation. Both of dialing, pulse and tone, are provided in this block. One important think about this design is compatibility with conventional telephone sets. according to diagrams of fig. 2, the telephone driver block writes or reads speech and signaling in RAM_SP or RAM_SIG memories respectively according to the east or west side.

Conference mode is supported in the OSC that a special number is dedicated for this mode and all users in sites can speak together. Fig. 3 illustrates how two voices are mixed together.

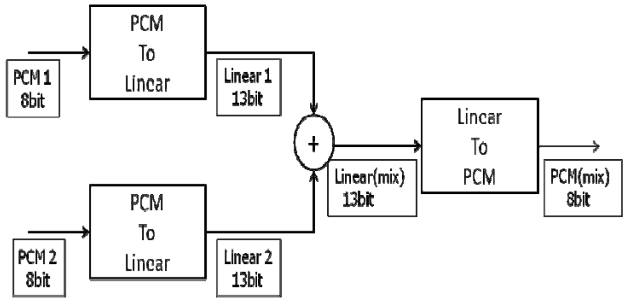

Fig. 3 mixing two voice signals

The output of CODEC is PCM, which is a kind of modulation in digital for voice. We cannot add 2 PCM's for mixing them. As can be seen in fig. 3, at first they should be converted to linear mode (13 bit) and added then the mixed linear voice is converted to PCM (8 bit).

B. Micro Interface

Micro interface block communicates data from CPU card to other DWDMs and vice versa. 29 slots of E1 frame allocate for data. Therefore, the throughput is 1856 kbps for data. This block writes data in FIFO_TX and reads data from FIFO_RX according to the sides.

All RAMs and FIFOs are implemented internally in the FPGA chip. And we don't use any external memory for the design.

C. E1 Transmitter and Receiver

E1 transmit block reads speech, signaling and data from the memories and then locates them in E1 frames. The block creates E1 format according to the G.703 and G.704 protocols. In other side, received E1 format is recognized by E1 receive block and it separates voice, signaling and data then writes in relative RAMs.

D. Manchester Coding and Decoding

In addition, Manchester code is performed in E1 out. Manchester code causes that we have 0 and 1 throughout the frame. So, the optical receiver doesn't saturate and clock recovery can be easy for receiver block.

IV. Manchester and NRZ Code Compare

Non-return to Zero (NRZ) and Manchester codes are used in digital systems to represent the binary values "1" and "0". Fig. 4 defines how NRZ and Manchester code represent binary values. NRZ is the code most often used. In NRZ, logic "1" is represented as a high level throughout a data cell, and logic "0" is represented by a low level. Manchester code represents binary values by a transition rather than a level. The transition occurs at mid-bit, with a low-to-high transition used to represent logic "0", and a high-to-low to represent logic "1".

Depending on the data pattern, there may be a transition at the cell boundary (beginning/end). A pattern of consecutive "1s" or "0s" results in a transition on the cell boundary. When the data pattern alternates between "1" and "0", there is no transition on the cell boundary.

In NRZ, only one level/data cell is required, while in Manchester, two levels are required. A DC component exists in NRZ when contiguous "1s" or contiguous "0s" are transmitted. When the data pattern alternates between "1s" and "0s", the frequency response is equal to 1/ 2 the clock rate. The frequency response for NRZ then ranges from DC to clock/2. The frequency response of Manchester code ranges from clock/2, occurring when the data pattern is alternating "1s" and "0s", to clock.

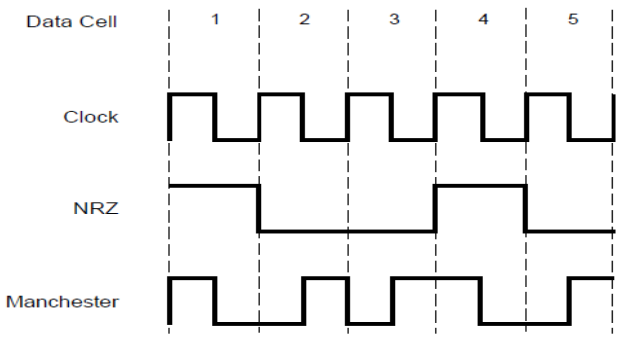

Fig. 4 Binary Values for NRZ and Manchester Codes

Two advantages of NRZ are that it does not require encoding/decoding, and it makes the most efficient use of a communication channels bandwidth. Manchester requires a modulation rate twice that of NRZ to transmit the same amount of information. This can be important in bandwidth limited communication channels. On the other hand, the receiver of NRZ requires a true DC response. Since, Manchester code has no DC component, it can be transformer coupled. The mid-bit transition in Manchester code provides a self-clocking feature of code. This can be used to improve synchronization over non-self clocking codes as NRZ. The transition also allows additional error detection to be done with relatively little circuitry.

In serial communication, clocks are used to define the size/boundary of a data cell. With a non self clocking code, since the clock and data are distinct, there can be skew between clock and data. In magnetic media applications, skew may be due to variations in the tape drive speed. In serial communication, skew results from differences in the transit delay between clock and data lines on long serial links.

One design objective in serial communication is to decode data correctly in the presence of noise, or an otherwise degraded signal. Signals have non-zero rise and fall times during which the signal value is indeterminate. In a receiver, sampling, or the decoding of the value of a signal, should occur as far from the signal transition as possible. Sampling at the time furthest from the signal transition is known as center sampling.

In a Manchester decoder, center sampling occurs at points 1/4 and 3/4 through the cell, since transitions occur always at mid-bit and sometimes on the cell boundary. In addition to center sampling, the receiver in a Manchester decoder does clock recovery. Since Manchester has transitions at least once each data cell, the receiver has known references to which it can resynchronize at each bit.

To synchronize to an incoming serial data stream, the receiving circuitry in a Manchester decoder can use a digital phase lock loop or a counter algorithm. Digital phase lock loops are most often used in networks with a ring topology while counter algorithms are common in point to point links

V. Error Detection

The most commonly used error detection schemes in serial communication are parity and cyclic redundancy check codes. When Manchester code is used, a small amount of additional circuitry can detect bit errors. Fig. 5 represents how the mid-bit transitions of Manchester code allow error detection.

Fig. 5 shows four rows of transmitted data, with the first row the valid Manchester representation for a logic "1". The three lower rows are waveforms of a corrupted form of the first row, and are erroneously transmitted data.

When Manchester data is shifted in serially into a shift register in the decoder, an exclusive OR can monitor for different values on each side of the data cell (since there is a mid-bit transition). With this error detection, an error is undetected only if each half of a data cell transitions from its original state.

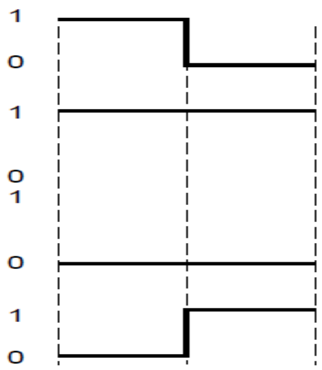

Fig. 5 Manchester Code Mid-bit Transitions

VI. Synthesis of the Design

We use Quartus II software for compiling of the design The Quartus II development software provides a complete design environment for system-on-a-programmable-chip design. Regardless of whether we use a personal computer or a Linux workstation, the Quartus II software ensures easy design entry, fast processing, and straightforward device programming. You can easily combine different types of design files in a hierarchical project, choosing the design entry format that works best for each functional block. The Quartus II Compiler provide powerful design processing that you can customize to achieve the best possible silicon implementation of your project. Automatic error location and extensive documentation on error and warning messages make design modifications as simple as possible. At every step in the design process, the Quartus II software makes it easy for you to focus on your design—not on how to use the software. All blocks in the plan are described by VHDL which is very strong language in FPGA design. The circuit is compiled and after synthesis, it implemented in a FPGA chip which is named EP2C5T144C8 of Cyclone II series from Altera Corporation. This chip is proper for this design and it provides requirements in speed and area features. Beside logic elements, it also has additional features such as memory bits and PLLs that are very practical for implementing the design. The results of compiled plan are shown in table 1.

TABLE I
FLOW SUMMARY OF COMPILING RESULTS

Item	Result
Quartus II Version	9.0 Build SJ Web Edition
Top-level Entity Name	OSC
Family	Cyclone II
Device	EP2C5T144C8
Timing Models	Final
Met timing requirements	No
Total logic elements Total combinational functions Dedicated logic registers	4017/4608 (87%) 3018/4608 (65%) 2655/4608 (58%)
Total pins	67/89 (75%)
Total virtual pins	0
Total memory bits	58560/119808 (49%)
Embedded multiplier 9-bit elements	0/26 (0%)
Total PLLs	1/2 (50%)

As it can be seen, the design has compiled in Quartus II version 9.0 and it uses 4017 logic elements (87%), 65% of total combinational function and 58% dedicated logic registers. It also consumes 67 pins (75%), 58560 memory bits (49%) and 1 PLL (50%). Since the circuit is used beside other DWDM circuits, the remained resources in the FPGA can be used for other circuits. The results are reasonable for the plan. Therefore we can use this controller with other circuits in one chip easily.

VII. CONCLUSION

This paper introduced OSC for DWDM system based on Manchester code and described some of the advanced features they incorporate. The system can accommodate a wide range of bit-rates, capacities, span lengths, span numbers, and as well as deploy Ethernet packet over TDM base OSC. The design is done by VHDL and according to the results show that the tasks of the design are satisfied and plane is optimized in using of area of FPGA chips.

ACKNOWLEDGMENTS

This work has been done as a part of contract 7831313 with Iran Telecommunication Research Center, Tehran, Iran. The author's wishes to thank ITRC organization for their kind support of project.

REFERENCES

[1] Fredette and J. P. Lang, "Link Management Protocol (LMP) for Dense Wavelength Division Multiplexing (DWDM) Optical Line Systems", Internet draft (work in progress), draft-ietf-ccamp-lmp-wdm-02.txt, 2003.

[2] S.V. Kartalopoulos, "Next Generation SONET/SDH: Voice and Data", Wiley/IEEE Press, 2004.

[3] Y. Li, D. Wang, and J. Li, ''FTTH remote fiber monitoring using optical wavelength domain reflectometry (OWDR) and wavelength coded tag (WCT),'' in Optical Fiber Commun. (OFC'06), 2006, Paper OThu3.

[4] H. Fathallah, and L.A. Rusch, ''Network management solution for PS/PON, WDM/PON and hybrid PS/WDM/PON using DS-OCDM,'' in Conf. Optical Fiber Communication (OFC), Paper OThE2, 2007.

[5] P. S. André, J. L. Pinto, A. L. J. Teixeira, M. J. N. Lima, J. F. da Rocha, Bit error rate assessment in DWDM transparent networks using optical performance monitor based in asynchronous sampling, OFC2002, 2002.

[6] E. Edmon, K.G. McCammon, R. Estes, J. Lorentzen, ''Chapter 2: Today's broadband fiber access technologies and deployment considerations at SBC,'' Broadband optical access and FTTH, ed. Chin-Lon Lin, Chap. 3, p17, (John Wiley & Sons, 2006).

[7] W. Hofmann, G. Gohm, M. Ortsiefer, E. Wong, and M.C. Amann, ''Uncooled High-Speed 1.55 um VCSELs for CWDM Access Networks,'' IEE European Conference on Optical Communications (ECOC), postdeadline paper Th4.5.4, Cannes, France, Sept. 2006.

[8] D.J. Shin, Y.C. Keh, J.W. Kwon, E.H. Lee, J.K. Lee, M.K. Park, J.W. Park, K.Y.Oh, S.W. Kim, I.K. Yun, H.C. Shin, D. Heo, J.S. Lee, H.S. Shin, H.S. Kim, S.B. Park, D.K. Jung, S. Hwang, Y.J. Oh, D.H. Jang, and C.S. Shim, ''Low-cost WDM-PON with colorless bidirectional transceivers,'' J. Lightwave Technol., vol.24, pp158–165, Jan. 2006.

[9] W. Lee, S.H. Cho, M.Y. Park, J.H. Lee, C. Kim, G. Jeong, and B.W. Kim, ''Wavelength filter detuning for improved carrier reuse in loop-back WDM-PON,'' Elect. Lett., vol.42, no.10, pp596–597, May 11, 2006.