Design of a High Performance T/R Switch for 2.4 GHz RF Wireless Transceiver in 0.13 μm CMOS Technology

Mohammad Arif Sobhan Bhuiyan, Mamun Bin Ibne Reaz

***Abstract*—** The rapid advancement of CMOS technology, in the recent years, has led the scientists to fabricate wireless transceivers fully on-chip which results in smaller size and lower cost wireless communication devices with acceptable performance characteristics. Moreover, the performance of the wireless transceivers rigorously depends on the performance of its first block T/R switch. This article proposes a design of a high performance T/R switch for 2.4 GHz RF wireless transceivers in 0.13 μm CMOS technology. The switch exhibits 1- dB insertion loss, 37.2-dB isolation in transmit mode and 1.4-dB insertion loss, 25.6-dB isolation in receive mode. The switch has a power handling capacity (P1dB) of 30.9-dBm. Besides, by avoiding bulky inductors and capacitors, the size of the switch is drastically reduced and it occupies only (0.00296) mm2 which is the lowest ever reported in this frequency band. Therefore, simplicity and low chip area of the circuit will trim down the cost of fabrication as well as the whole transceiver.

***Keywords*—** CMOS, ISM band, SPDT, t/r switch, transceiver.

I. Introduction

THE rapid advancement of CMOS technology, in the recent years, has led the scientists to fabricate wireless transceivers fully on-chip which results in smaller size and lower cost wireless communication devices with acceptable performance characteristics [1-3]. Therefore, the current trend is to design low power compact devices by eliminating bulky board level off-chip components [4-5]. Utilizing the advantages of unlicensed 2.4 GHz band, demand of wireless devices such as RFID, Bluetooth, Zigbee and Wi-Fi devices, non-contacting medical instruments, sensors etc. are increasing day by day. The sizes and performances of such devices mainly depend on the sizes and performances of their transceivers. Therefore performance enhancement of such wireless transceivers is a crying need of time [6-8].

An efficient T/R switch is an essential component of every concurrent wireless transceiver. It helps the transceiver to share a single antenna for both transmission and reception modes providing adequate isolation between themselves [9], [10]. In the receive mode, the T/R switch ties the antenna to the receiver offering high impedance path to the transmitter; whereas, in the transmit mode, the switch ties the antenna to the transmitter and imposes large impedance to the receiver as shown in figure 1.

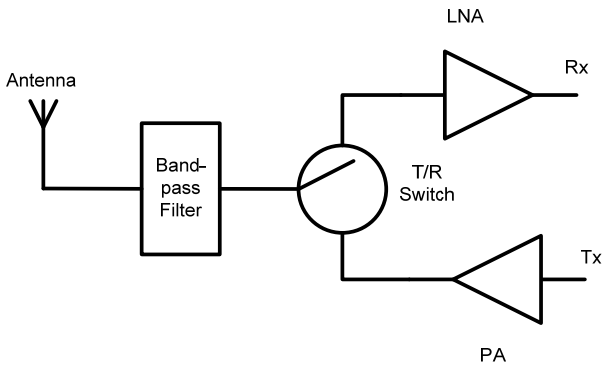

Fig. 1. SPDT T/R switch and matching network at the transceiver front end.

The architecture of a T/R switch should be such that it exhibits less insertion loss, high isolation, large power handling capacity, low offset, and tiny switching time along with adequate reliability [11-12]. But In practical design, the trade-off among themselves cannot be overlooked at a given frequency band [13]. For silicon CMOS switches this trade-off becomes prominent especially in 2.4 GHz ISM band [14]. Several series-shunt T/R switch in this band have been reported in literatures and most of the works emphasized on a single performance parameter.

Figure 2 shows the basic circuit diagram of series-shunt T/R switch architecture. Addition of two shunt arms to the series-type T/R switch leads to the shunt/series-type T/R switch. A complement control signal, Vc and Vc′, is applied at the gate of the transistors, M1 and M2, to alternate the ON/OFF states in the same way as in the series type switch. The series transistors, M1 and M2, execute the main switching task while the shunt transistors, M3 and M4, provides low-impedance paths for the unwanted signals to the RF ground. Therefore, the two shunt

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arms make the T/R switch have relatively better isolation between transmitter and receiver port compared to previous type switch. Although the isolation is improved in series-shunt switch but insertion loss of the switch is also found to become deteriorated at higher frequencies [15].

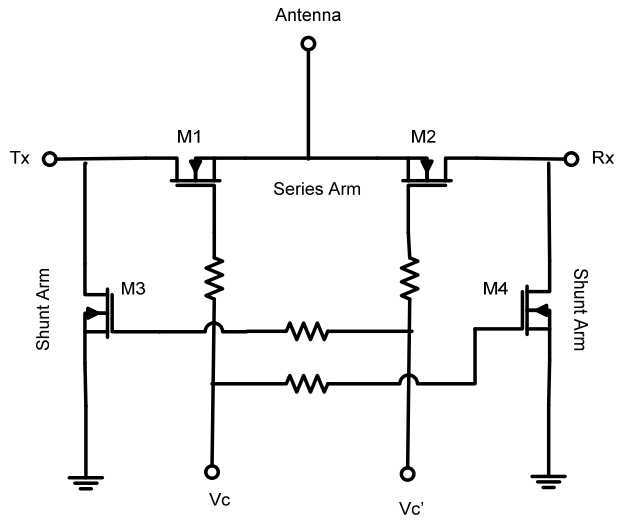

Fig. 2. Typical Series-shunt T/R switch topology.

Yamamoto et al. (2001) demonstrated the basic consideration for improvement of performance of typical series-shunt type T/R switch by only optimizing the gate width of the transistors [16]. Therefore that design exhibited low isolation and low power handling capacity. Besides, due to the usage of large transistors, the size of the chip was large. To improve the performance, Huang (2001) adopted DC biasing technique along with optimization of transistor gate width in his design which resulted in low insertion loss along with moderate isolation and power handling capacity [17]. The size of the chip was also reduced to a half which is still large compared to present circuits.

In the year 2004, Huang (2004) and Hove et al. (2004), introduced impedance transformation and parasitic MOSFET model, respectively, to improve the isolation and insertion loss of the switch [18] [19]. But both of them could not reduce the size of the switch. Yeh et al. (2006) utilized the resistive body floating technique to improve the overall performance of the switch but the P1dB and isolation of the switch was not adequate for high power transceivers. But they reduced the size drastically [20].

In this article, a series-shunt type T/R switch in 0.13 µm CMOS technology is demonstrated for 2.4 GHz ISM band applications especially for IEEE 802.11b/g/n transceivers. In this design, proper optimization of transistor width - length and resistive body floating technique is utilized to enhance the overall performance of the switch keeping the circuit architecture simple. Utilizing such high performance T/R switch, efficient and reliable transceivers can be manufactured for different low-cost wireless appliances and therefore, industry as well as individuals will be highly benefited.

II. METHODOLOGY

The schematic circuit of the proposed series-shunt T/R switch topology is illustrated in Figure 3. Complement control signals, Vc and Vc´, are applied at the gate terminals of the transistors (M1, M2, M3, M4, M5 and M6) to alternate their ON/OFF states. An inverter, consists of (M7 and M8), does the job of inverting the control voltage. The control voltages are applied through gate resistances (RG1-RG6) to minimize the consequence of capacitive coupling around the gates of the OFF transistors [21]. The series transistors (M1 and M2) execute the original switching task while the shunt transistors (M3 M4, M5 and M6) provides low-impedance paths for the unwanted signals to the RF ground. Therefore, the shunt arms make the T/R switch obtaining relatively better isolation between the transmitter and the receiver port but at the cost of insertion loss.

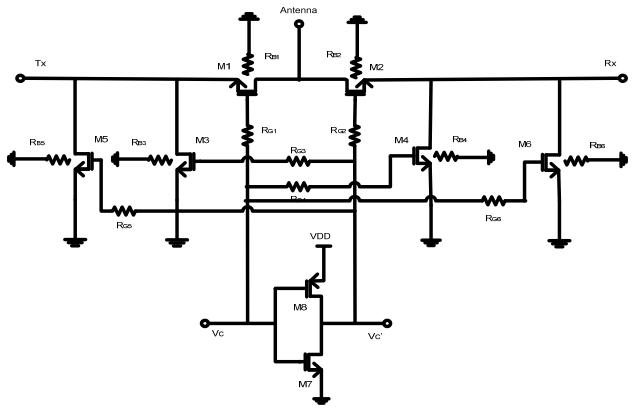

Fig. 3. Schematic circuit of proposed series-shunt SPDT T/R switch.

During the transmit mode, a high control voltage Vc (1.8 V) is applied at the gate of transistors (M1, M4 and M6) while control voltage Vc´ at the gates of (M2, M3 and M5) is kept low (0 V). As a result, the signal from the transmitter (power amplifier) is sent to the antenna and any signal leaking through M2 toward the receiver (Low noise amplifier) is shunted by the transistors M4 and M6. The vice-versa is true for receive mode.

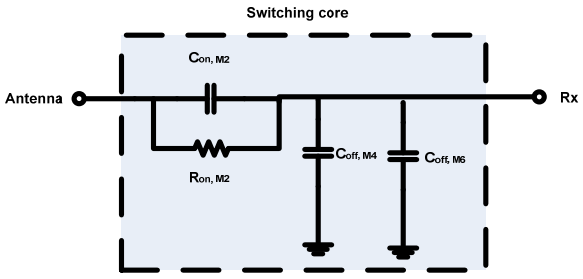

Fig. 4. Abridged equivalent circuit of the proposed T/R switch at receive mode.

Figure 4 shows the equivalent circuit of the proposed T/R switch, in the receive mode. To understand the effect of resistances and capacitances on the circuit, insertion loss property of the T/R switch has been analysed numerically for receive mode. For this analysis, the transistor M2 is considered to be biased within the linear region whereas the transistors M4 and M6 are kept in cut-off mode.

Insertion loss of an RF switch evaluates its small signal power loss during the ON state of the switch. The insertion loss of a switch is inversely proportional to the S21 parameter of the core of the switch.

Body floating technique is essential for improving power handling of the switch. This technique reduces the signal loss through the junction diodes between source/drain and body of the transistor [24-25]. Usually, the body of a transistor is tied to its source and its equivalent circuit. As long as the input power to the transistor remains small, the transistor becomes nonconducting and it turns off. However, as the input power is made to increase, the drain to source voltage becomes negative and forward biases the diode between the drain terminal and the body. As a result, the input impedance of the NMOS becomes lower. But if the body floating technique is adopted, the body of the MOS is tied with the ground with a high resistance. Therefore, it retains high input impedance of the transistor to maintain better power performance of the switch [20]. The gate resistances are used to provide DC bias isolation at the gates. These resistances are used to mitigate the voltage fluctuations around the gate terminal which can affect the channel resistance as well as can cause breakdown at the gate terminal. Moreover, in order to keep the switching speed of the transistor, choosing suitable gate bias resistor is very important. So, we used 5 KΩ resistors for body floating (RB1-RB6) and 5 Ω for gate biasing (RG1-RG6). The circuit elements utilized in this architecture and their values are given in Table I.

TABLE I
T/R SWITCH ELEMENTS AND ITS VALUES

ELEMENTS	VALUE
M1 – M8	100/0.13 (μm/μm)
RG1 – RG6	5 Ω
RB1 – RB6	5 Ω

III. RESULTS AND DISCUSSION

The proposed T/R switch is designed and simulated in 0.13-μm CMOS process by using a transient analysis within Mentor Graphics design architect IC (DA-IC). Figure 5 shows the isolation and insertion loss of the switch for 802.11b/g/n band and it is clear that the values of the isolation and insertion loss for this band remain constant which are 37.2 dB and 1 dB respectively.

Figure 6 and Figure 7 show the insertion loss and isolation of the switch for both transmit and receive mode in perspective of input power (Pin). The insertion loss of the switch in both modes is found to increase exponentially with input power. The isolation is found to decrease steadily in both cases. At P1dB point the values of the insertion loss and isolation are 1.0 dB (Tx mode) and 1.4 dB (Rx mode) and 37.2 dB (Tx mode) and 25.6 dB (Rx mode), respectively.

Reliability is a big performance issue for every circuit. It is very important for a circuit to determine how long it can maintain its performance to an acceptable limit if the process variables, e.g. temperature, are changed. Figure 8 illustrate that with an increase in temperature both the insertion loss and isolation of the proposed switch increase. For a 125°C temperature variation the variations in insertion loss and isolation are 0.16 dB and 2 dB respectively.

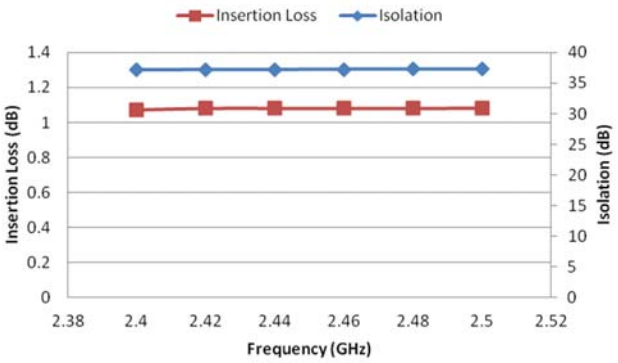

Fig. 5. Insertion loss and Isolation of the switch.

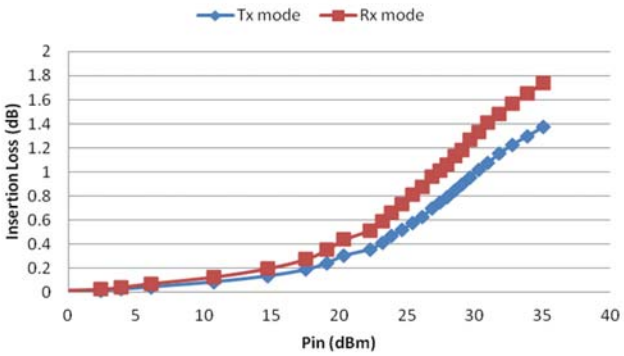

Fig. 6. Insertion loss of the switch at Tx and Rx mode.

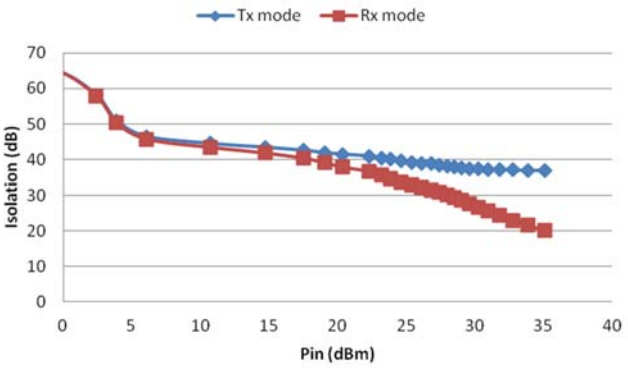

Fig. 7. Isolation of the switch at Tx and Rx mode.

The proposed switch can handle large amount of power during transmission mode with a very small insertion loss and better isolation of receiver circuit. This characteristic is very essential because the higher the isolation the more reduced amount of power loss from the transmitter to the receiver which is directly related to transmitter efficiency. Besides as the receiver circuit handle very small amount of power, therefore, higher isolation protects the receiver from being got damaged by high transmitted power. The low insertion loss makes the switch suitable for high performance transceiver front end and therefore, enhances transmitter efficiency. Furthermore, the high power handling capacity of the switch makes it reliable for

larger signal transmission with adequate linearity. On the other hand, low insertion loss and high isolation is vital for reception mode because the receiver handles very low amount of power. The high insertion loss degrades the receiver output whereas low isolation demeans the noise figure of the receiver. Moreover, low switching time is crucial issue especially for high frequency applications for both transmission and reception stage.

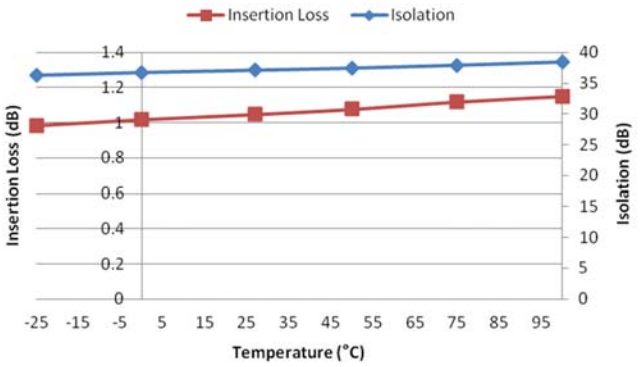

Fig. 8. Insertion loss and isolation of the switch with temperature variation at 2.4 GHz band.

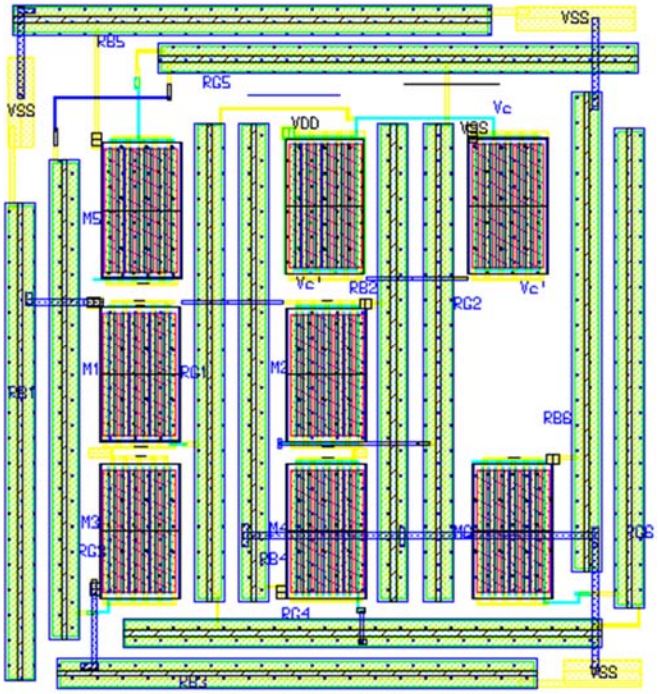

Fig. 9. Layout design of the proposed switch (0.0526x0.0564) mm2.

Therefore 1- dB insertion loss, 37.2-dB isolation and 30.9-dBm power handling capacity in transmit mode and 1.4-dB insertion loss, 25.6-dB isolation in receive mode with extremely low power dissipation and low switching time makes the switch appropriate for related application. For the entire 2.4 GHz band these values remain constant with constant temperature, but varies by a little amount with the temperature and thus it is reliable too. Moreover the switch occupies only 0.00296 mm2 of IC space, as illustrated in Figure 9, which is lowest ever reported in this frequency band. A comparison of this work to the recently reported performances of 2.4 GHz CMOS switches is given in Table II.

IV. Conclusion

Fully integrated T/R switches have several advantages over the discrete switches or the switches those use off-chip components. The design of a fully on-chip 2.4 GHz T/R switch in 0.13µm CMOS technology has been reported. The results exhibit 1- dB insertion loss, 37.2-dB isolation and 30.9-dBm power handling capacity in transmit mode whereas 1.4-dB insertion loss, 25.6-dB isolation in receive mode with extremely low power dissipation. Body-floating technique and proper transistor optimization help the proposed switch attaining low insertion loss, high isolation, faster switching speed, good power performance and linearity simultaneously. Besides the chip area of the switch is reduced drastically by avoiding bulky inductors and capacitors in the circuit.

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TABLE II
UNITS FOR MAGNETIC PROPERTIES

Ref.	Year	CMOS Process	Vc/Vc´ (volts)	Isolation (dB)	P1dB (dBm)	IL (dB)	Area (mm^2)	Comments
[16]	2001	0.18-µm	1.8/0	24	11	1.5	0.45 *	Optimizing gate width
[17]	2001	0.18-µm	6.0/2.0	24.4	17	0.8	0.28	Optimizing transistor widths and dc biasing
[19]	2004	0.35µm	3.6/0	42	16	1.3	0.026	Parasitic MOSFET model
[18]	2004	0.18 µm	6.0/2.0	20.6	20.6	1.1	0.28	Impedance transformation
[25]	2006	0.18-µm	1.8/0	35	21.3	0.7	0.03	Body-floating
[26]	2008	0.5µm	1.2/0	-	25.33	1.085 (Tx) 1.102 (Rx)	-	DC biasing
This work	2014	0.13 µm	1.8/0	37.2 (Tx) 25.6 (Rx)	30.9	1.0 (Tx) 1.4 (Rx)	0.00296	Optimizing gate width and body floating